

Title: Improved Voltage Segmented Digital to Analog Converter

Related Applications

This application claims the benefit of U.S. Provisional Application Serial Number 60/458,907, filed on March 28, 2003.

Background

The invention relates generally to digital to analog converters (DACs) and, more particularly, relates to an improved voltage segmented DAC that requires no buffer.

Digital converters (DACs) are well known in the art, and are configured to convert a digital signal to a voltage, or an analog signal. In high speed or high resolution applications, conventional DACs suffer from their complexity bulkiness as a result of a large number of components, and often lack linearity.

Voltage segmented DACs are a conventional approach to this problem, and are configured with multiple stage resistor strings. In one example, a segmented DAC is configured in two stages with separate resistor strings that resolve two sets of digital bits, higher order and lower order bits. It has been observed, however, that the application of secondary or successive voltage segmenting elements has perturbed the precise operation of the primary or preceding elements. This configuration and other similar conventional approaches require a buffer or amplifier to isolate the secondary and successive voltage segmenting elements from the primary or preceding elements. Buffers and amplifiers add a large number of components to a circuit, and affect the speed and accuracy of operation of the circuit.

Therefore, there exists a need for an accurate DAC, but that does not require a buffer. As will be seen, the invention provides such a DAC in an elegant configuration.

Brief Description of the Drawings

The invention is illustrated by way of example and not limitation in the figures of the accompanying drawings. The same numbers are used throughout the figures to reference like components and/or features.

FIG. 1 is a schematic diagram of an improved segmented DAC according to the invention; and

FIG. 2 is a more detailed schematic diagram of an improved segmented DAC according to the invention.

Detailed Description

An improved segmented digital to analog converter is provided having a first segment with a series of resistors and configured to receive and convert one set of digital bits of the input signal to an analog signal. The converter further has a second segment
5 configured to receive and convert a second set of digital bits from the input signal to an analog signal. The second segment has a second series of resistors configured to receive the second set of digital bits of the input signal. The second segment has a first current source connected at one end of the second series of resistors, and a second current source
10 connected at another end of the series of resistors. In operation, a current is transmitted between the two current sources to substantially remove error from the digital bits received in the form of a digital signal received at the second segment.

The invention is directed to an improved segmented digital to analog converter
15 configured with a novel method of compensating current flow in secondary or successive segmented elements. In operation, dual current devices initially load, then subsequently unload a cascade of resistor networks connected to the secondary or successive voltage segmenting elements, preventing the perturbation of precise operation of the primary or preceding elements. The improved converter removes substantially all errors from the
20 secondary or successive cascade of connected resistor networks, and does not substantially disturb the circuit as a whole. In contrast to conventional approaches, the improved converter obviates the need for a buffer or amplifier to isolate the secondary and successive voltage segmenting elements from the primary or preceding elements. Clearing out errors existing in the secondary or successive elements serves to prevent
25 errors that would previously cause errors in the primary or preceding elements, obviating the need for isolation of the secondary or successive elements.

In one embodiment, a segmented digital to analog converter is provided having an input for receiving an input signal and an output for outputting an analog output signal. A first segment is configured to receive and convert one set of digital bits of the input signal to an analog signal. A second segment is configured to receive and convert a second set of digital bits of the input signal to an analog signal, where the second segment has a series of resistors configured to receive the second set of digital bits, a first current source connected at one end of the series of resistors, and a second current source connected at another end of the series of resistors. In operation, current is transmitted between the first and second current source in a manner that substantially removes error in the transmission of the second set of digital bits. The current transmitted between the first and second current source is performed in a manner that substantially removes error in the transmission of the second set of digital bits without creating a disturbance in the circuit as a whole.

Referring to Figure 1, a novel segmented DAC 100 configured according to the invention is illustrated. The elements 126 of figure 1 are one means by which a digital signal may be accepted into the DAC – elements within 126 are not the subject of this disclosure and are included only to illustrate one example of a digital connection scheme. One conventional digital connection scheme is used on the Analog Devices AD569: a voltage segmented DAC. The DAC is configured as a 16 bit DAC, and the processing is separated into the eight most significant bits, and the eight least significant bits. The invention is not limited by the number of bits the DAC is configured to process, but extends to any size DAC.

The DAC includes a most significant bit (MSB) segment selector 102 configured to process the eight most significant bits of a sixteen bit input, and further includes a least significant bit (LSB) segment tap selector 104 configured to process the eight least significant bits of the sixteen bit input. Preceding selector 102 is a cascading bank of resistors 106. This bank of resistors is configured to receive a positive voltage V_{hi} and a negative voltage V_{lo} thereby defining the range of the DAC to voltages between V_{lo} and V_{hi} . Selector 104 is connected to a cascaded resistor bank 116. The

upper and lower voltages of this cascade of resistors 116 are set by nodes 118 and 120 respectively.

As the 8 bit number 122 is changed the nodes 118 and 120 are connected to successive taps on the primary resistor chain 106. The voltages on nodes 118 and 120 represent the first 8 bit subdivision of the DAC range defined by the voltages on nodes 108 and 110. The design intention is that the second resistor cascade 116 will further subdivide the voltage between 118 and 120. Within the base segment selector 102, it may be desirable to use FET switches, or FET devices configured to operate as simple switches. By this means, the node 118 is connected to a node emerging from 106 and 120 is connected to a node typically one tap below that node where 118 is connected.

It will be obvious to those skilled in the art that such a connection would cause a current to flow out of node 118 and into node 120, that current being the current flowing in the secondary resistor chain 116. Thus, without benefit of the invention, an error voltage is present in the first resistor chain 106. It is known in the art that a buffer or amplifier taking essentially zero input current may be interposed between nodes 118, 120 and the secondary chain 116 to obviate this problem. However it is also well known that such a buffer amplifier has its own problems, where the offset voltage contributes an error and the finite bandwidth increases settling time. A circuit configured according to the invention removes the loading error without use of a buffer amplifier.

The innovation lies in the use of a current that is pushed into and then taken out of the subsidiary resistor strings using the current devices 128, 130. This operation is performed in such a manner that the voltage across the subsidiary string of resistors is already substantially equal to the voltage across the segments where it will be connected by the action of the switches. Referring to Figure 2, one means is illustrated by which that current may be made, namely by biasing the first resistor network between low impedance points of a current source and deriving a scaled version of that current from a parallel connection of PMOS and NMOS devices. It will be evident to those skilled in the art that other means to create this current are possible without departing from the spirit and scope of the invention.

Referring to Figure 2, an improved segmented DAC 200 is illustrated in accordance with the invention. The first set of eight resistors 202 is connected between

low impedance nodes 204, 206 as shown. In operation, this creates a voltage from end to end on the bank of resistors 202 that is divided into eight equal voltages. The voltage is made available via the set of switches 208, shown here as 8 switches numbered 0-7, controlled by the bus "A" 210 to the second set of resistors 212.

5 In conventional systems, this second set of resistors 212 would, if connected by the switches 208, be expected to cause an error. That error would be that the resistors 212 would in effect lower the incremental resistance of the resistor, for each corresponding resistor of resistor bank 202 to which the second bank is connected, across which they connected, thus disturbing the voltage across it. However, according to the
10 invention, the expedient of providing a current from device 214 into the top and removing the same current from the bottom of this second set of resistors with current device 216 is sufficient to substantially remove this error. This result may be seen and better understood by consideration of the superposition of currents. The ideal current that the second set of eight resistors must take in order to have the ideal voltage across them is
15 simply one eighth of the current flowing in the first resistor chain. There are eight secondary resistors of the same value as the first eight resistors. They have only $1/8^{\text{th}}$ of the voltage across them, hence $1/8^{\text{th}}$ of the current through them. In conventional circuits, this current would have to flow out of the first resistor chain, thus disturbing it. However, in the improved circuit illustrated in Figure 2, and according to the invention,
20 the devices 214 and 216 each form part of a cascoded current source providing this current. Hence no current needs to flow out of the first set of resistors. Hence there is no disturbance. This is the principle and may be repeated again for a third set of resistors and can be repeated for successive sets of resistors (not shown). In this circuit there is substantially no systematic error resulting from operation. Given that the currents are
25 accurate, the error is substantially zero and independent of the resistance of the switches in the "on" or closed position used to connect the second set of segmented elements to the first set of segmented elements. This is also true for a second set connected to the third set, and other successive sets that may be connection in other circuits.

Those skilled in the art will understand that it is possible that error may occur, but
30 any error that may be present in any practical circuit is nominal. For example, assume

that the error in the second resistor string current (that provided by 214 and removed by 216) is say 1%. This error is substantial, but the true question is whether the error will cause disturbance in the system. Upon observation, it will be evident to those skilled in the art that the maximum error occurs at the maximum impedance of the center tap,
5 which is at the halfway point. This impedance is $N \cdot R/4$, where N is the number of resistors in series for each segmented resistor bank, eight in the example illustrated in Figure 2, and R is the elemental resistance in the example of Figure 2. The error is thus $(0.01 \cdot V / (N \cdot R)) \cdot (N \cdot R/4)$, or only $0.0025 \cdot V$. Thus, the error is suppressed by a factor of 4, or two digital bits.

10 Examples as described pertain to audio signal processing. It will be appreciated, however, that this is illustrative of only one utility of the invention, and that the invention has greater applicability. It will be appreciated by those skilled in the art that the invention is applicable to any type of digital signal processing technology including but not limited to acoustic signal processing, image signal processing, and multi-dimensional
15 signal processing, without departing from the spirit and scope of the invention, which is defined in the appended claims and their equivalents.